77-79 Ghz Stacked Low Noise Amplifier for Automotive Radar

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Abstract

This paper presents the design of a three stage stacked low noise amplifier for automotive radar applications. Stack structure is employed to overcome the inability of MOSFETs to operate at high voltage levels, as stacked MOSFETs can tolerate $k \times V_{max}$ where V_{max} can be chosen to be near the breakdown voltage of a single device. Realized in 65nm CMOS process, the stacked amplifier provides a gain of 15 dB with noise figure of 3.5 dB at 79 GHz. The amplifier draws 28.2 mA current from a 3V supply. To examine the nonlinear behavior of the amplifier Volterra analysis is performed, second and third order harmonic distortions are determined. The effect of feedback on the output resistance is examined using Blackman's analysis. Sensitivity analysis of the stacked LNA is also performed to determine the effect of parameter variations on the circuit performance.

Key Words: Stack amplifiers, Low Noise Amplifiers, Volterra analysis

1. Introduction

Radio frequencies from 30 GHz to 300 GHz have wave length from ten to one millimeter called millimeter wave (mm-wave).The mm-wave spectrum is gaining the attention of researches because of the advantages available at higher frequencies. Trend of escalating frequencies is due to the fact that higher data rates can be achieved along with less power consumption [1].Moreover, on chip antenna integration can also be achieved [2], so recently there is a surge of mm-wave integrated circuits, demand and popularity of mm-wave systems is increasing in civil and military applications. Consumer demand for 60 GHz and above applications is expected to increase over millions of products produced and sold in 2015 [3].

Being the first active stage of any receiver frontend, low-noise amplifier (LNA) design plays a vital role in the overall performance of any receiver. LNA is responsible for providing gain to the weak incoming signals from the antenna with minimum added noise and distortion. On the other hand it should be able to provide a decent gain for the strong incoming signals with good linearity. Therefore the main design concerns for the LNA design are gain, noise figure and linearity.

The frequency band of 77 GHz to 81 GHz was allocated by the European Commission (EC) for the automotive short range radar systems. 79 GHz automotive radar equipment is now authorized in most of European Union (EU) countries [4]. Automotive radar systems are installed on the vehicles to assist the driving safety. This system provides information regarding other vehicles and obstacles present on the road.

Design of RF circuits is challenging task and the question before today's researcher is which circuit topology and which process technology to be used although the choice of technology and topology is badly affected by the monitoryfactors but yet the choice has to made from variety of circuit topologies and process technologies available.

Most common LNA topologies presented in literature are common source (CS), common gate (CG), cascade, cascode and differential low noise amplifiers. Other configurations like variable gain low noise amplifier (VGLNA), electrostatic discharge (ESD) protected LNA, transformer feedback LNA and current reuse LNAs are also reported.

In this paper, a 79 GHz LNA is presented which is designed specifically to be utilized in 79 GHz automotive radar system. The low-noise amplifier is realized using 65nm CMOS process with three stage stacked topology as the stacked topology provides better saturated output power which is desirable in case of automotive radar application.

2. Stacked-FET Amplifier

The schematic of an n-stacked amplifier is shown in Fig. 1. The circuit consists of common-source (CS) FET transistor cascaded with common gate (CG) like FETs. In stacked FET configuration, CG like transistor experiences a voltage swing however in cascode configuration,

the gate of CG transistor is grounded at the desired frequency of operation. The upper FET in cascode configuration presents a low input resistance to the lower FET, causing the small voltage gain for the lower FET, which reduces the Miller feedback capacitance from the lower FET's drain to gate. This loss of voltage gain is recuperated by the upper FET. Unlike cascode configuration small gate capacitance (C_2, C_3 etc.) is introduced at the gate of each stacked transistor to allow voltage swing. The value of external capacitance is so chosen that the voltage divider formed due to gate-to-source capacitance (C_{gs}) and external capacitance C_n produce an in-phase voltage swing at gate and drain.

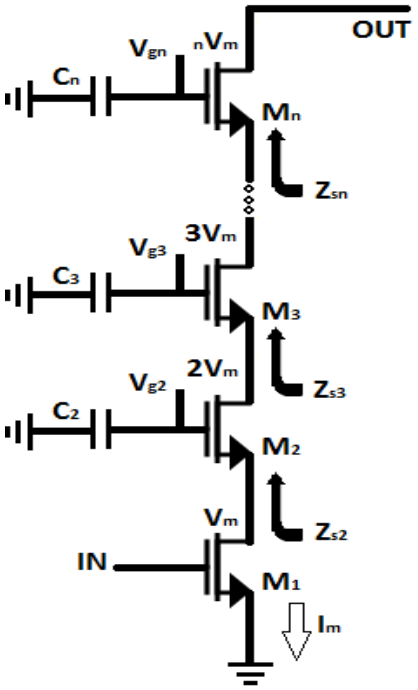

Fig. 1: n-Stacked FET configuration

The series combination of external gate capacitance (C_2,C_3,...C_n) and gate to source capacitance (C_{gs2},C_{gs3},...C_{gsn}) of the FET form a voltage divider network, this network reduces the drain – gate and drain – source voltage under large signal conditions, permitting Stacked configuration to be realized as more reliable configuration for large voltage swings Gain of stacked FET amplifier is less than that of cascode but higher saturated output power and drain efficiency is a tradeoff for that reduced gain [5].

Fig. 2 shows the small signal equivalent circuit of FET with external gate capacitance C. The source impedance of the FET is influenced by the external gate capacitance. Equation (1) describes the dependence of source impedance Z_s.

$$Z_s = (1 + \frac{C_{gs}}{C})(\frac{1}{g_m} // \frac{1}{sC_{gs}}) \quad (1)$$

The small signal voltage gain of the stacked amplifier configuration can be derived as.

$$A_v = \frac{g_{m1} R_L}{\left(1+\frac{sC_{gs2}}{g_{m2}}\right)\left(1+\frac{sC_{gs3}}{g_{m3}}\right)\ldots\left(1+\frac{sC_{gsn}}{g_{mn}}\right)} \quad (2)$$

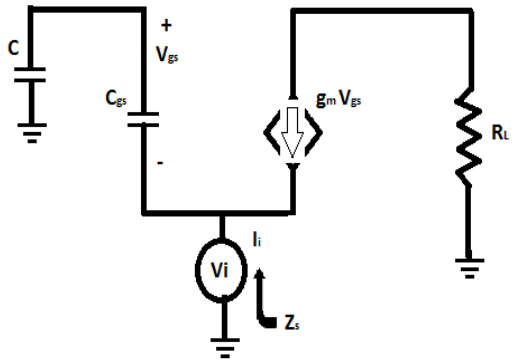

Fig. 2: External gate capacitance effect on FET's source impedance.

For the frequencies much lesser than the cutoff frequency of the device being used the impedance ($Z_{s2}Z_{s3}$. . .Z_{sn}) of the device is approximately resistive[6]. All the devices will share the same current I_m. However at higher frequencies the reactive component of the load impedances ($Z_{s2}Z_{s3}$. . .Z_{sn}) due to C_{gs} becomes significant and degrades the gain as can be seen from equation (2). All the devices will experience different current due to current leaking out through C_{gs}.

We can adjust C_{gs} by adjusting the W/L ratio of the transistors used in the design.

Table 1: Comparison of stacked and parallel FET configurations[6]

Parameter	n-stacked FET	n-Parallel FET
Peak drain current	I_m	$n\, I_m$
Peak drain voltage	$V_m n$	V_m
Input capacitance	C_g	$n\, C_g$
Output impedance	$\frac{n\, V_m}{I_m}$	$\frac{V_m}{n\, I_m}$
Output power	$\frac{1}{8} V_m n\, I_m$	$\frac{1}{8} V_m n\, I_m$
Voltage gain	$g_m n \frac{V_m}{I_m}$	$g_m \frac{V_m}{I_m}$

Table 1 compares some important parameter of the n-parallel and n-stacked FET's configurations. Compared to n-parallel FET configuration the n-stacked configuration has n time greater voltage and power gains. Input and output impedances are also n times and n^2 times higher, results in better input and output impedance matching and less power loss in matching networks [6].

Above mentioned considerations and discussion makes the stacked FET configuration a strong candidate for LNA design.

3. Stacked-FET Low Noise Amplifier Design

Fig.3 shows the schematic of three stage stacked low noise amplifier. The circuit is composed of common source (CS) stage connected in cascade with two common gate like stages. The Stacked LNA is optimized to operate at 77-79 GHz, the frequency range allocated for automotive radar applications.

A critical design consideration for every amplifier is its biasing which determine its efficiency and reliability. In stacked amplifier configurations where bias voltages are much greater than the break down voltages of the device, the DC and RF voltages of the devices in stacked configuration must be adjusted in such a way that it must not exceed the break down voltage of the individual device. The circuit shown in Fig. 3 is biased with independent voltage source at the gate of each device. The circuit draws 28.2mA from a 3V supply.

Fig.5shows the s-parameters for the three stacked LNA. Maximum power gain of 15dB is achieved at 79 GHz. Input output reflection coefficients along with reverse voltage gain is also shown in Fig.5.All transistors used in Fig.3are 65nmlongand 120µm wide.

Stacked topology provides better input and output impedance matching as compared to the cascade topology [5]. Capacitor $C_1$is representing pad capacitance, capacitors C_1, C_2, $C_3$and inductor L_1forms the input matching network. The minimum voltage standing wave ratio (VSWR) of 1.5 is achieved at the input side and the magnitude of VSWR is 1.6 on the output side as can be seen from Fig.6. The value of VSWR on the input and output side is well below the acceptable value of two. Input and output VSWR can also be calculated using the equations (3) and (4).

$$\text{Input VSWR} = (1 + |S_{11}|)/(1 - |S_{11}|) \quad (3)$$

$$\text{Output VSWR} = (1 + |S_{22}|)/(1 - |S_{22}|) \quad (4)$$

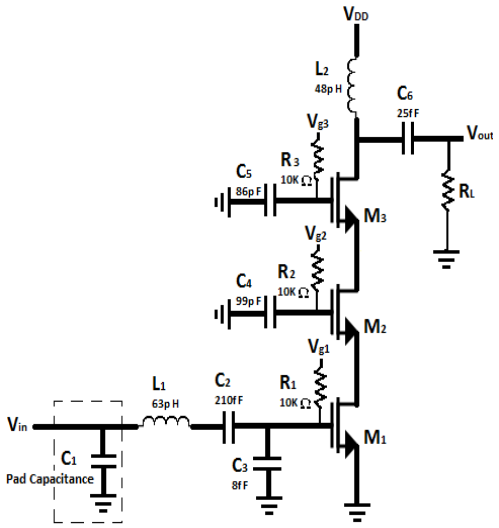

Fig. 3: Schematic of three stacked LNA

The value of external gate capacitances are so chosen that eliminates the need for intermediate node matching components presented in [16]. The source impedance of the FETs in stack configuration depends on the external gate capacitance as described by equation (1). Thus by adjusting the external gate capacitance, the source impedance of the FET can be adjusted for impedance matching between the stages to eliminate the need for intermediate node matching components.

Noise Figure (NF) is one of the important parameter to be considered while designing the LNAs [7]. Fig.7 shows the NF of the purposed three stacked LNA. Minimum NF of 3.5 dB is achieved at 78GHz; however NF increases rapidly after the desired frequency of 79 GHz. Designing a low noise amplifier requires a trade-off between the gain and the noise figure. It is important to mention here that minimum noise figure does not necessarily occur at either system impedance or at conjugate match impedance that maximize the gain. The noise figure defined in terms of noise factor (F) can be presented by the following equation.

$$NF = 10\log_{10} F \quad (5)$$

$$F = F_{min} + \frac{4R_n}{Z_o}\left(\frac{|\Gamma_{opt} - \Gamma_s|^2}{|1+\Gamma_{opt}|^2(1-|\Gamma_s|)^2}\right) \quad (6)$$

Where

F_{min} =Minimum noise factor

R_n = Equivalent noise resistance

Z_o = System impedance

Γ_{opt} = Optimum source reflection coefficient

Γ_s = Source reflection coefficient

F_{min}, R_n and Γ_{opt} are often referred as noise parameters. Fig.4 shows the noise circles, here minimum noise factor is achieved at optimum source reflection coefficient.

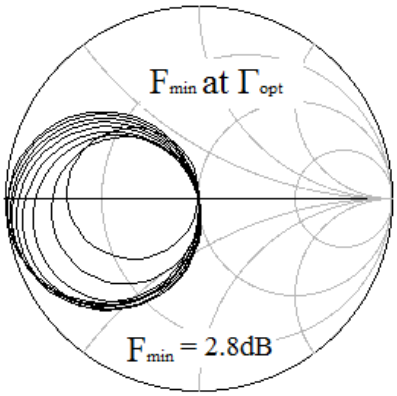

Fig. 4: Noise Circles

For the circuit to be unconditionally stable, the stability factor (K) should be greater than one. For K less than one the circuit will be potentially unstable and oscillations may occur with certain combination of source and load impedance [8]. Circuit presented in this paper is found to be highly stable. Fig. 8 is the graph between stability factor and the frequency, it can be seen that the value of K is well above one. Theoretically the value of K can be determined using the equation (6).The purposed stacked LNA is highly stable because the CS stage acts like a degenerative component for the other CG like stages.

$$K = \frac{1+|D_s|^2-|S_{11}|^2-|S_{22}|^2}{2\,|S_{21}|^2|S_{12}|^2} \qquad (7)$$

Where

$$D_s = S_{11}S_{22} - S_{12}S_{21} \qquad (7)$$

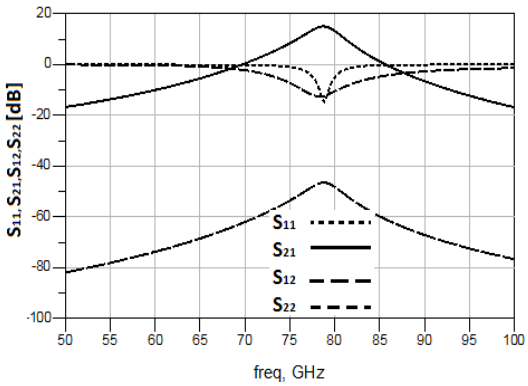

Fig. 5: S-parameters for the 77-79 GHz three stacked LNA.

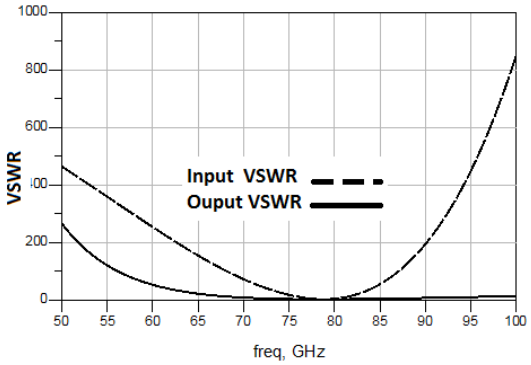

Fig. 6: VSWR for the 77-79 GHz three stacked LNA.

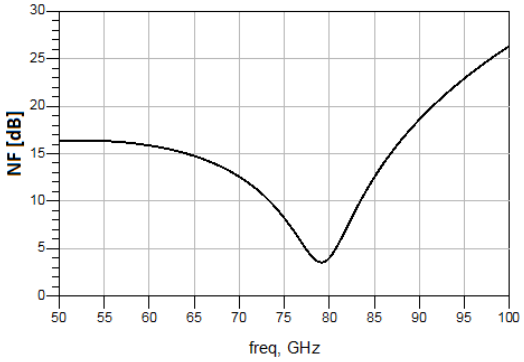

Fig. 7: Noise Figure for three stacked LNA.

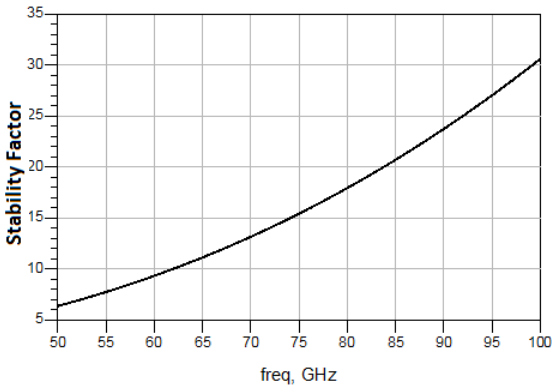

Fig. 8: Stability Factor of three stacked LNA.

The amplifier is designed to handle large input signal levels, as the performance requirement from the circuits used in automotive radar applications become critical when the signals are coming from some nearby source. The 1dB compression point is 3.9 dBm, as shown in Fig.9.The compression point can be further shifted to the right side of the graph by increasing the bias current ultimately putting an upper limit on the value of 1-dB compression point [7]. The equation (8) shows how the 1-dB compression point is related to the current.

$$P_{1-dB} = \frac{I_{peak}\,(V_{DD}-V_{DS,Saturation})}{2} \qquad (8)$$

The third order input intercept point (IIP3) is shown in Fig.10. Generally IIP3 is kept 10-dBm higher than 1-dB compression point. High IIP3 requires higher current drawn while lowest NF is possible at lower currents [9]. The purposed stack amplifier is biased with 28.2mA current to maintain both, the desired level of IIP3 and gain. The IIP3, OIP3 and gain are interrelated terms, equation below describes these relations.

$$IIP3 = P_{IN} + \frac{\Delta P}{2} \quad (9)$$

Where

$$\Delta P = P_{out} - P_{out2}$$

$$P_{out} = Power\ at\ first\ order$$

$$P_{out2} = Power\ at\ second\ order$$

Also

$$IIP3 = OIP3 - G \quad (10)$$

Where $G = gain$

From the equation (9) it can be seen that to increase the level of IIP3 it is desirable to have a low level of P_{out2} and from the equation (10) it is clear that higher gain will cause IIP3 to drop.

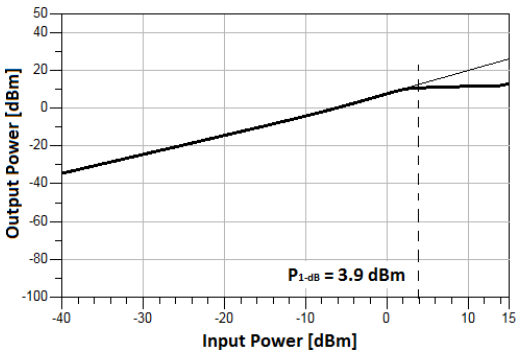

Fig. 9: 1-dB compression point curve

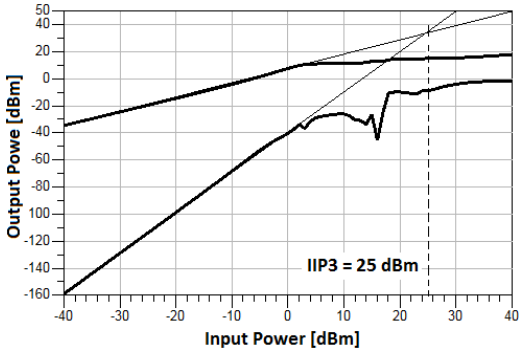

Fig. 10: IIP3 curve

4. Volterra series analysis

Volterra series analysis is a popular technique for analyzing the weakly nonlinear behavior of the circuits. Volterra series describes the output of nonlinear system as sum of first order operator, a second order operator, a third order operator and so on [15]. The block diagram representation of these operators is shown in Fig. 11.

$$Y(t) = H_1[x(t)] + H_2[x(t)] + H_3[x(t)] + \cdots + H_n[x(t)] \quad (11)$$

$$H_n[x(t)] = \int_{-\infty}^{+\infty} \dots \int_{-\infty}^{+\infty} h_n(\tau_1, \tau_2, \dots \tau_n,) x(t-\tau_1) x(t-\tau_2) \dots x(t-\tau_n) d\tau_1 d\tau_2 \dots d\tau_n \quad (12)$$

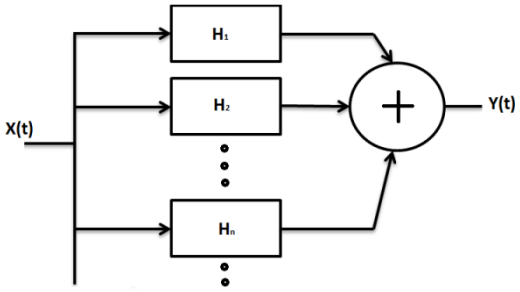

Fig. 11: Volterra series representation of a nonlinear system

Equation (11) and (12) describes the relationship between input and output of a nonlinear system. In this representation H_n is n-th order Volterra operator.

Second and third order harmonic distortion analysis of the circuit purposed in Fig.3 is performed using Volterraseries, equation (13) and (14) are the general expression for determining the second and third order harmonic distortions.

$$HD_2 = \frac{V_{in}}{2}\left|\frac{2(J\omega_1, J\omega_1,)}{H_1(J\omega_1)}\right| \quad (13)$$

$$HD_3 = \frac{{V_{in}}^2}{4}\left|\frac{H_3(J\omega_1, J\omega_1, J\omega_1)}{H_1(J\omega_1)}\right| \quad (14)$$

Overall transfer function of the circuit shown in Fig.3 is represented by the equation (15).

$$A_v = \frac{g_{m_1} g_{m_2} g_{m_3} sC_2 R_1 R_L}{(sC_{gs_2} + g_{m_2})(sC_{gs_3} + g_{m_3})(s^3 W + s^2 X + sY + sZ + 1)} \quad (15)$$

Where $C_2C_3L_1R_1 = W, L_1C_2 = X, C_2R_1 = Y, C_3R_1 = Z$

Equation (16) is the transfer function of the overall linear circuit and Equation (17) is the gain of the amplifier shown in Fig. 3. Equation (18) and (19) are the second and third order kernel transforms.

Equation (20) and (21) are the expression for the harmonic distortion, coefficients $K_{2A}$and

$K_{3A}$are referred as second and third order nonlinearity coefficients. Fig. 11 and 12 are the representation of the second and third order harmonic based on equations (20) and (21).

From the harmonic distortion equations it can be observed that the harmonic distortion is dependent on the input matching network as well as the transconductance of the FETs plays an important role.

Fig. 14-15 are the transconductance gain vs. seconds order harmonic distortion curves; g_{m1} is the major contributor of the second order harmonic distortion. As g_{m1} is the transconductance of the input FET and the major contributor of the gain as can be seen from equation (2) it can be concluded that the harmonic distortion can be reduced by reducing the gain of the amplifier. Fig. 16-17 are the curves between transconductance and HD_3. Similar results can be drawn for the HD_3 that is drawn for HD_2.Fig. 18 is the IBias vs. gain curve which shows that the gain of the amplifier increases with the bias current to a certain level and then degrades. As bias current is affecting the gain and gain is affecting the HD2 and HD3, IBias can be adjusted to a level to achieve desired HD2 and HD3.

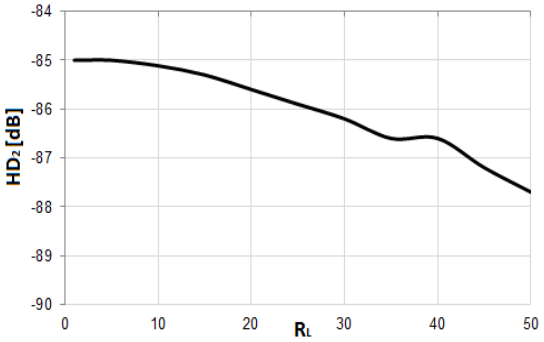

Fig. 12: Effect of RL on HD2

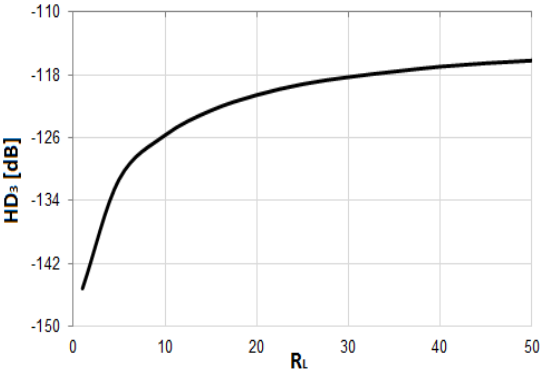

Fig. 13: HD3 variation with RL

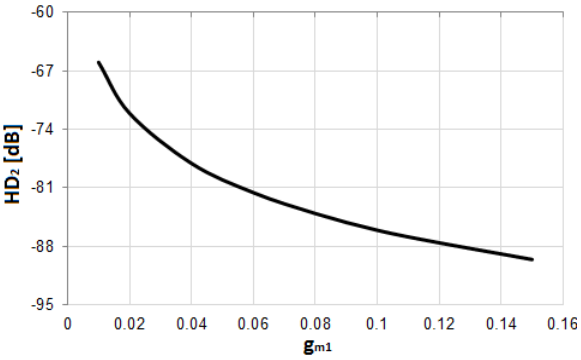

Fig. 14: gm1 vs. HD2 Curve

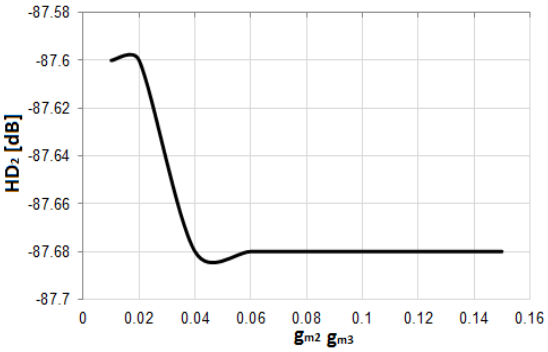

Fig. 15: gm2 and gm3 vs. HD2 Curve

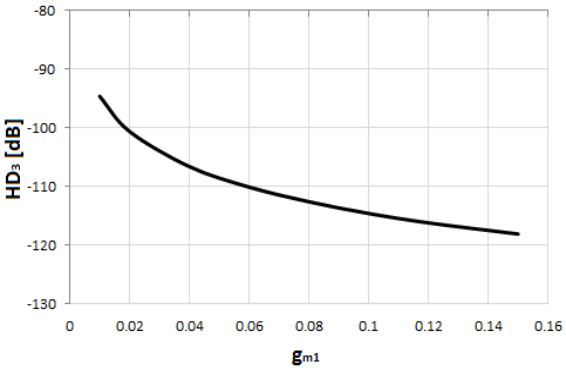

Fig. 16: gm1 vs. HD3 Curve

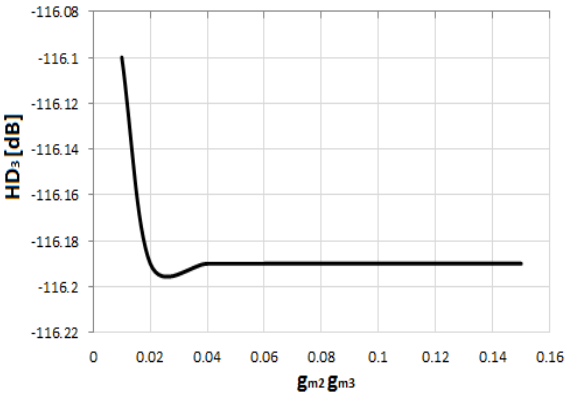

Fig. 17: gm2 vs. HD3 Curve

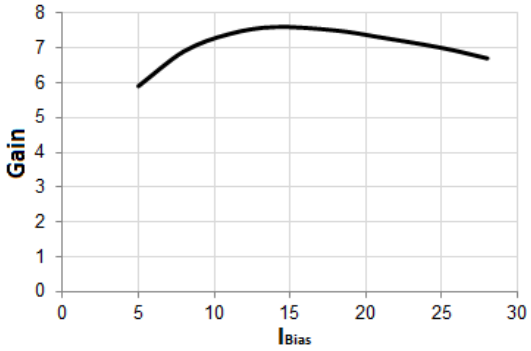

Fig. 18: Gain vs. IBias

$$H_1(j\omega_1) = \left[\frac{g_{m1}g_{m2}g_{m3}}{(j\omega_1 C_{gs2}+g_{m2})(j\omega_1 C_{gs3}+g_{m3})}\right]\left[\frac{j\omega_1 R_1 C_2}{j\omega_1{}^3 C_2C_3L_1R_1+j\omega_1{}^2 C_2L_1+j\omega_1(C_2R_1+C_3R_1)+1}\right]R_L \quad (16)$$

$$A=\frac{g_{m1}g_{m2}g_{m3}}{(j\omega_1 C_{gs2}+g_{m2})(j\omega_1 C_{gs3}+g_{m3})} \quad (17)$$

$$H_2(j\omega_1, j\omega_2) = K_{2A}\left[\frac{j\omega_1 R_1 C_2}{j\omega_1{}^3 C_2C_3L_1R_1+j\omega_1{}^2 C_2L_1+j\omega_1(C_2R_1+C_3R_1)+1}\right]\left[\frac{j\omega_2 R_1 C_2}{j\omega_2{}^3 C_2C_3L_1R_1+j\omega_2{}^2 C_2L_1+j\omega_2(C_2R_1+C_3R_1)+1}\right]R_L \quad (18)$$

$$H_3(j\omega_1, j\omega_2, j\omega_3) = K_{3A}\left[\frac{j\omega_1 R_1 C_2}{j\omega_1{}^3 C_2C_3L_1R_1+j\omega_1{}^2 C_2L_1+j\omega_1(C_2R_1+C_3R_1)+1}\right]\left[\frac{j\omega_2 R_1 C_2}{j\omega_2{}^3 C_2C_3L_1R_1+j\omega_2{}^2 C_2L_1+j\omega_2(C_2R_1+C_3R_1)+1}\right]\left[\frac{j\omega_3 R_1 C_2}{j\omega_3{}^3 C_2C_3L_1R_1+j\omega_3{}^2 C_2L_1+j\omega_3(C_2R_1+C_3R_1)+1}\right]R_L \quad (19)$$

$$HD_2 = \frac{V_{in}}{2}\cdot\frac{K_{2A}}{A}\left|\frac{j\omega_2 R_1 C_2}{j\omega_2{}^3 C_2C_3L_1R_1+j\omega_2{}^2 C_2L_1+j\omega_2(C_2R_1+C_3R_1)+1}\right| \quad (20)$$

$$HD_3 = \frac{V_{in}{}^2}{4}\cdot\frac{K_{3A}}{A}\left|\left[\frac{j\omega_2 R_1 C_2}{j\omega_2{}^3 C_2C_3L_1R_1+j\omega_2{}^2 C_2L_1+j\omega_2(C_2R_1+C_3R_1)+1}\right]\left[\frac{j\omega_3 R_1 C_2}{j\omega_3{}^3 C_2C_3L_1R_1+j\omega_3{}^2 C_2L_1+j\omega_3(C_2R_1+C_3R_1)+1}\right]\right| \quad (21)$$

5. Blackman Analysis

Blackman's formula is a popular method of calculating the impedance of feedback networks. As conventional techniques depend on the identification of the type of feedback network employed to determine the impedance, Blackman's formula dispenses with that requirement. To obtain the results with Blackman's formula one has to put the values into the formula and solve. For a circuit shown in Fig.19 the Blackman's impedance can be written as.

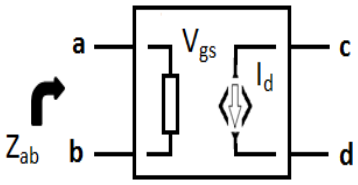

Fig. 19: Feedback Network

$$Z_{ab} = Z_{ab}^0\left(\frac{1+(T_{sc})_{ab}}{1+(T_{oc})_{ab}}\right) \quad (22)$$

Where

Z_{ab}: Impedance seen at the terminal a-b when the feedback network is working normally

Z_{ab}^0: Impedance seen at the terminal a-b with g_m=0

$(T_{sc})_{ab}$: Return ration for the short circuit terminals a-b

$(T_{oc})_{ab}$: Return ration for the open circuit terminals a-b

Let us consider a three stage stacked amplifier shown in figure (a). To determine the feedback impedance Z_{out} of the amplifier at the terminal "output" using Blackman's impedance formula, a small circuit equivalent of the stacked amplifier shown in Fig.20 is drawn.

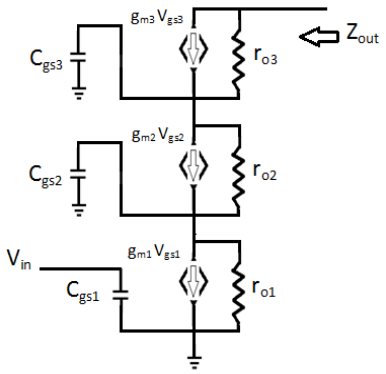

Fig. 20: Small Circuit equivalent of three stage stacked amplifier

In order to find the impedance using Blackman's impedance formula one has to determine all the components of the Blackman's formula i.e. Z_{out}^0,$(T_{sc})_{out}$and $(T_{oc})_{out}$.

In order to find Z_{out}^{0} we have to set g_m=0, the resultant circuit is shown in figure 3.

The value of Z_{out}^{0} can be represented by the equation (23)

$$Z_{out}^{0} = [\{(r_{o1}||C_{gs2}) + r_{o2}\}||C_{gs3}]||r_{o3} \quad (23)$$

To determine $(T_{sc})_{out}$ the dependent source has to be changed with independent source and then return ratio has to be determined. Fig.22 shows the circuit used to determine the$(T_{sc})_{out}$.

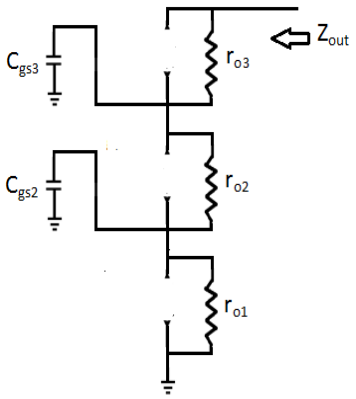

Fig. 21: Small circuit equivalent circuit of three stage stacked amplifier with gm=0

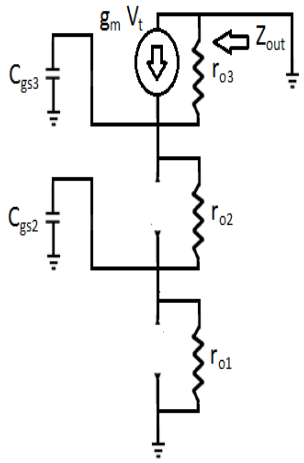

Fig. 22: Small signal equivalent circuit used for Blackman analysis

$$(T_{sc})_{out} = (r_{o1}||C_{gs2})\left[\frac{r_{o3}||C_{gs3}}{[(r_{o1}||C_{gs2})+r_{o2}]+[r_{o3}||C_{gs3}]}\right]g_m \quad (24)$$

$(T_{oc})_{out}$is found to be zero.

Now as we have the values for all the components of Blackman's formula, the impedance Z_{out}can be found using the following equation.

$$Z_{out} = [\{(r_{o1}||C_{gs2}) + r_{o2}\}||C_{gs3}]||r_{o3} \times 1+(r_{o1}||C_{gs2})\left[\frac{r_{o3}||C_{gs3}}{[(r_{o1}||C_{gs2})+r_{o2}]+[r_{o3}||C_{gs3}]}\right]g_m \quad (25)$$

6. Sensitivity Analysis

While designing any electronic circuit it is important to know the effect of system parameter variations on its performance. Any performance parameter change caused due to change in one or more circuit parameters is referred as circuit sensitivity.

Let $H(s)$ be the function of any circuit, and x be the parameter associated with some circuit element, the sensitivity$S_x^H(s)$ of the function $H(s)$ with respect to circuit parameter x, assuming all other circuit parameters are constant, is defined as

$$S_x^H(s) = \frac{\partial H(s)}{\partial x}.\frac{x}{H(s)} \quad (26)$$

Equation (26) is the expression for normalized sensitivity where

$$H(s) = \frac{V_{out}}{V_{in}} \quad (27)$$

Here $H(s) = A_v$

Circuit parameter x is called critical if its sensitivity with respect to $H(s)$ is high. By sensitivity analysis the effect of parameter change on the circuit performance can be analyzed, as the circuit parameters keeps on changing due to aging and temperature variations of the surroundings.

Table 2: Sensitivity table

Circuit Component (Parameter)	Sensitivity Value
L_1	.135
C_2	.043
C_3	.091
R_1	.0023
R_2	0
R_3	0
g_{m1}	1
g_{m2}	.0071
g_{m3}	.007Z1

Sensitivity analysis of the circuit shown in Fig.3 is performed and the sensitivity values are presented in table 2. Equations (28)-(36) are the simplified sensitivity equations for the parameters given in table 2. The equation (28) is the sensitivity equation for the inductor L_1, as the sensitivity is determined with respect to gain the sensitivity value of L_1 is reflecting how the gain will be affected due to change in the value of inductor L_1. Similarly the effect of other circuit components on the gain can be observed from the

table 2. The circuit shown in Fig. 3 is not sensitive for the resistors R_2 and R_3. .The most sensitive circuit parameter is found to be g_{m1} with sensitivity value of one.

$$S_{L_1}^{H}(s) = -\frac{s^2L_1C_2(sC_3R_1+1)}{s^3C_2C_3L_1R_1+s^2C_2L_1+sC_2R_1+sC_3R_1+1} \quad (28)$$

$$S_{C_2}^{H}(s) = \frac{sC_3R_1+1}{s^3C_2C_3L_1R_1+s^2C_2L_1+sC_2R_1+sC_3R_1+1} \quad (29)$$

$$S_{C_3}^{H}(s) = -\frac{sR_1C_3(s^2C_2L_1+1)}{s^3C_2C_3L_1R_1+s^2C_2L_1+sC_2R_1+sC_3R_1+1} \quad (30)$$

$$S_{R_1}^{H}(s) = \frac{s^2C_2L_1+1}{s^3C_2C_3L_1R_1+s^2C_2L_1+sC_2R_1+sC_3R_1+1} \quad (31)$$

$$S_{R_2}^{H}(s) = 0 \quad (32)$$

$$S_{R_3}^{H}(s) = 0 \quad (33)$$

$$S_{g_{m1}}^{H}(s) = 1 \quad (34)$$

$$S_{g_{m2}}^{H}(s) = \frac{sC_{gs2}}{sC_{gs2}+g_{m2}} \quad (35)$$

$$S_{g_{m3}}^{H}(s) = \frac{sC_{gs3}}{sC_{gs3}+g_{m3}} \quad (36)$$

7. Monte Carlo simulations

Monte Carlo simulation approach can also be used to determine the effect of parameter change on circuit performance Monte Carlo analysis is essentially a statistical analysis technique; it provides the statistical data predicting the effect of randomly varying model parameters on the output within specified tolerance limits.

All the circuit performance parameters are important however Monte Carlo analysis of the gain with respect to different circuit parameters is performed.

Fig.23 is the Monte Carlo simulation of the purposed circuit shown in Fig.3 with respect to the gain and the gain variations are observed only with respect to inductor L_1variations. Inductor is considered to have ±2% tolerance. The thickness of the curve shown in Fig.23 is representing the possible outcomes of gain values with randomly varying ±2% inductor L_1. For a ±2% inductor the value of gain varies from 14.6 dB to 12.5 dB at 78 GHz.Fig. 24-26is the Monte Carlo analysis curves for the gain with respect to capacitor C_2, C_3, and resistor R_1 respectively. All the components are considered to have ±2% tolerance, and the thickness of the curve is the possible outcome of the gain with respect to C_2, C_3, and R_1variations.

The performance comparison of the proposed LNA with other amplifiers is given in table 3.

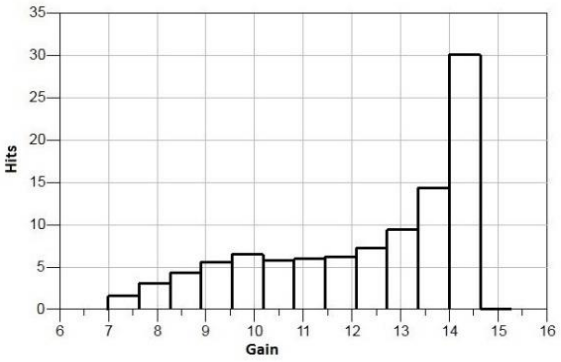

Fig. 23: Monte Carlo simulation for L1

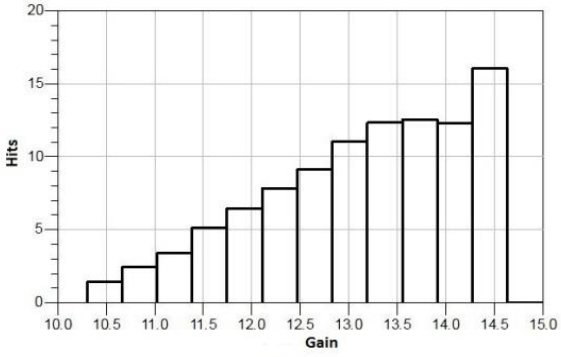

Fig. 24: Monte Carlo simulation for C2

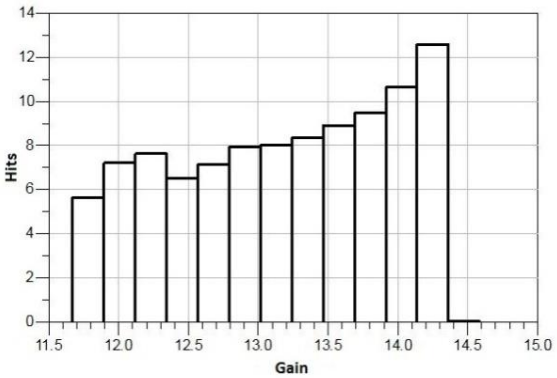

Fig. 25: Monte Carlo simulation for C3

8. Frequency Compensation

Frequency compensation techniques are widely used to improve the stability and bandwidth of amplifiers.

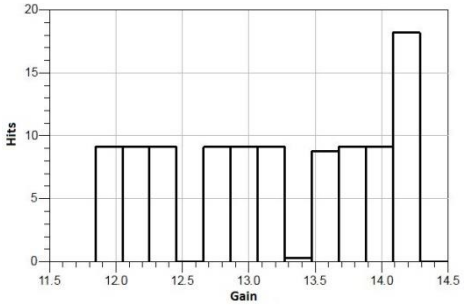

Fig. 26: Monte Carlo Simulation for R1

Table 3: Performance comparison of different LNA configurations

References	**Frequency GHz**	**Technology**	**Topology**	**Gain dB (Max)**	**Noise figure dB**	**POWER DISSIPATION mW**	**P-1dB**
This work	79	65nm	3 stage stack	15	3.5	84.6	3.9
[16] 2015	45	45nm	3 stage stack	6.2			
[14] 2014	77-81	90nm	3 Cascaded stages	13	6.2	21.1	-
[5] 2013	46	45nm	3 stage Stack	9.4	-	-	-
[13] 2012	60	65nm	2 stage Cascade	12.2	6.5	-	-
[12] 2012	60	90nm	4 cascaded	12.5	5.4-6.5	4.4	-16
[11] 2011	61.2	65nm	Cascode stage with two staggered cascode stages	18.9-7.9	<13.9	45	-22.3-11.2
[10] 2011	58.5–73	65 nm CMOS	CS+ 2 Cascode	21.5	4.2	36	-22.1

Many compensation techniques have been reported i.e. Simple Miller compensation (SMC), Multi path Zero Cancellation (MZC), Nested Miller Compensation (NMC) to achieve better performance from the amplifiers. Most of these techniques are based on pole splitting and pole-zero cancellation using capacitors and resistors.

Simple miller compensation technique is applied to the circuit shown in Fig.3. SMC apart from moving the poles to the lower frequencies has additional advantage of moving non-dominant pole to higher frequencies. This pole splitting requires a capacitor to be connected from output to the input.

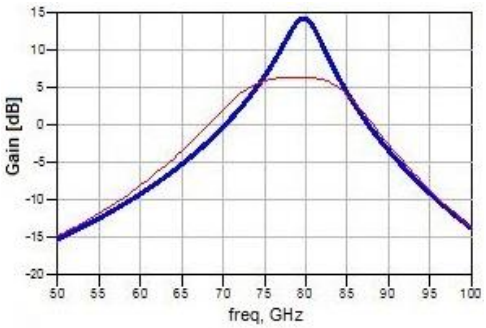

Fig. 27: Gain Vs Frequency graph after compensation

Fig. 27 shows the graph between gain and frequency after frequency compensation. From the figure it can be seen that broad banding is achieved at the cost of gain.

9. Layout

The layout of the purposed 77-79 GHz three stacked LNA is shown in Fig. 27, area is found to be 55.1 µm × 22.22 µm.

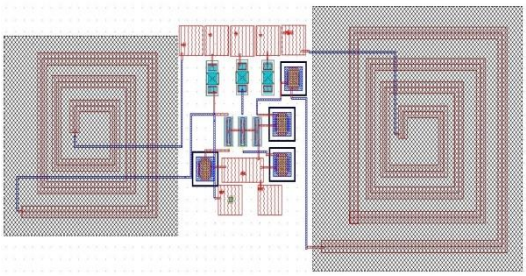

Fig. 28: Layout of the Purposed Three stacked LNA

10. Conclusion

A 3 stage stacked LNA realized in 65 nm CMOS for automotive radar application is presented. The circuit performance is optimized at 77-79 GHz frequency band. The proposed LNA shows 15 dB voltage gain, 3.5 dB NF at the middle of operating band of 77 GHz while dissipating 34.3mA from 3 V supply. Volterra analysis of the purposed LNA is also performed to determine the effects of nonlinearities. Blackmans analysis is performed to determine the effect of

feedback. Sensitivity analysis and Monte Carlo simulations are also performed. The proposed LNA can be adopted for automotive radar receiver.

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